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ART-UNIT: 234

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ABSTRACT:

A system and method for reprogramming a non-volatile memory of one or more on-board vehicle computers through a serial communication link between an off-board controller and the on-board vehicle computer. An interface circuit is also provided on the vehicle in order to process the command signals from the portable controller which will enable the non-volatile memory to receive and store new computer program code. The method follows a predetermined transfer protocol which assists in preventing the existing computer program code stored in the non-volatile memory from being improperly erased or re-written. This transfer protocol includes the transmission of a command signal from the off-board controller which has a voltage level that exceeds the voltage level of any signal which may recognized on the serial communication link.

16 Claims, 10 Drawing figures

Exemplary Claim Number: 1

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Brief Summary Text - BSTX (10):
Specifically, on-board vehicle computer **programs are stored** in one or more types of non-volatile **ROM,** which stands for "Read-Only Memory". **ROM** circuits come in various types, such as permanent circuits (**ROM**), programmable circuits (**PROM**), erasable-programmable circuits (**EPROM**) or electrically erasable-programmable circuits (**EEPROM**). Each of these **ROM** circuits are produced in the form of a semiconductor integrated circuit (IC) or circuit "chip" which may be separately mounted to a circuit board or contained in a larger chip that includes other circuits as well.

Brief Summary Text - BSTX (11):
With a permanent **ROM,** the computer **programs** are hard-wired into the chip during the manufacture of the chip, and the **program** cannot be changed. With a **PROM,** the computer **program** is electronically inserted or injected into the chip after it has been manufactured. The **EPROM** is like a **PROM** except it has the added capability of erasing the entire computer **program stored** in the chip by irradiating the chip with ultra-violet light for a period of time on the order of 20 minutes. Once the **program** is erased, then another computer **program** may be inserted into the chip to take its place. The **EEPROM** is

similar to the EPROM in that it permits erasure and subsequent re-programming. However, with an EEPROM, the entire computer program need not be erased, and the erasure may be accomplished very rapidly (e.g., 1-2 seconds) through the application of electrical signals.

Brief Summary Text - BSTX (13):
As will be appreciated from the above discussion of ROM memories, each of these memory types present different options when it is desired to update, revise or expand upon the computer programs which are stored in the memory chip. With permanent ROMs and PROMs, the chip itself has to be removed from the circuit board and replaced with a new memory chip which contains the desired computer programs. With an EPROM, the memory chip still needs to be removed from the circuit board in order to be erased. However, the EPROM chip may then be replaced on the circuit board after the new program has been injected into the chip.

Brief Summary Text - BSTX (14):
Due to the amount of time, labor and possible replacement costs involved in these procedures, none of these three types of ROM chips present particularly attractive options for applications where it may be desirable to periodically update the software stored on the memory chip. In contrast, EEPROMs and flash memories do offer a potentially viable option for updating or otherwise replacing existing software. In this regard, it is generally not necessary for a EEPROM or flash memory chip to be removed from a circuit board in order to erase all or part of a computer program and subsequently re-program the

appropriate memory cells. Additionally, as discussed above, the entire erasure/**reprogramming** procedure for these memory chips may be carried out very quickly.

Brief Summary Text - BSTX (23):
Under the method according to the present invention, the on-board vehicle computer is first initialized into a bootstrap mode, and then a **program** is down-loaded from the diagnostic tool to identify the on-board vehicle **flash** memory manufacturer and version of the computer **program** code currently residing in the non-volatile memory. Once it is determined that it is appropriate to **reprogram** this non-volatile memory with the computer **program** code contained in the plug-in module of the diagnostic tool, the existing computer **program** code in the non-volatile memory of the on-board vehicle computer is preferably erased. In one form of the present invention, a unique command signal is required to permit the erasure to proceed. This particular command signal is processed by the interface circuit on the vehicle to ultimately generate a **reprogramming** signal voltage level which is otherwise available on the vehicle. After the existing computer **program** code is erased, then the new computer **program** code from the plug-in module is immediately transmitted to the non-volatile memory of the on-board computer circuit via the communication link with the vehicle's signal transfer structure and the on-board computer.

Drawing Description Text - DRTX (9):
FIG. 7 is a perspective view of a wiring harness which forms part of the serial communication link when the non-volatile **flash** memory of the

transmission controller is to be **reprogrammed**.

Detailed Description Text - DETX (10):
As may be seen in FIG. 2, the **flash** memory chip Z179 is connected to the microprocessor chip Z144 through an address/data bus 101 (AD0-AD7), and an address bus 102 (A8-A14). The **flash** memory chip Z179 is also connected to the microprocessor chip Z144 through a plurality of control lines (E, R/W, A15), and a set of logic gates (NAND gates Z135, and invertor gate Z181). Thus, for example, control line A15 forms part of the address bus of the microprocessor chip Z144, and this particular line is used to enable the **flash** memory chip Z179 to receive signals from the other control lines. In this regard, it will be appreciated that the R/W control line will provide a signal for causing the **flash** memory chip Z179 to enter either a **write** mode or read mode. Similarly, the E control line is used to provide a clock signal to the **flash** memory chip Z179 from the microprocessor chip Z144. In this particular embodiment, the microprocessor chip Z144 is a Motorola 68HC11 microprocessor and the **flash** memory chip Z179 is a Toshiba 32Kx8 **flash** memory. However, it should be appreciated that other suitable microprocessor and **flash** memory chips may be utilized in the appropriate application.

Detailed Description Text - DETX (13):
Referring first of interface section 112, this circuit is used to detect and process a 12-volt bootstrap command signal from the diagnostic unit 28. This 12-volt bootstrap command signal is used to initiate a bootstrap mode within the microprocessor chip Z144 as an initial step under the method according to the present invention. In this regard, the 12-volt

bootstrap command signal is sent to the vehicle 10 via the serial communication channel 104 when the engine ignition is off. Subsequently, when the ignition is turned on, the microprocessor chip Z144 will "wake up" in the bootstrap mode. In the bootstrap mode, the microprocessor chip Z144 will execute a bootloader **program** and look for data on the SCIRX receive line, rather than receive the instructions previously **stored in the flash** memory chip Z179. In this way, control of the microprocessor chip Z144 is turned over to the computer **program** instructions **stored** in the plug-in module 32 of the diagnostic tool 28; whereas, the microprocessor chip Z144 would normally receive its instructions from the computer **program stored in the flash** memory chip Z179.

Detailed Description Text - DETX (16):

When the **reprogramming** signal is present on the SCIRX receive line, the transistor Q331 will conduct or turn on and permit the voltage level of this signal to be applied to the regulator Z101 via line 120. The regulator Z101 is designed to produce a very precise 12-volt output signal which is communicated to the Vpp port of the **flash** memory chip Z179 via line 122. The presence of the 12-volt output signal from the regulator Z101 will unlock the **flash** memory chip Z179 and enable the microprocessor chip Z144 to read the identity of the manufacturer of the **flash** memory chip. The presence of the **reprogramming** signal will also subsequently permit the existing computer **programs stored in the flash** memory chip to be erased. Thus, it should be appreciated that even though the **flash** memory chip Z179 may be controlled by the application of a 12-volt signal, the interface section 110 of the present

invention requires the
presence of a unique signal before the 12-volt voltage level will be applied to
the **flash** memory chip. It should also be noted that FIG. 2 shows a 68HCO5C4
coprocessor chip Z064 which is connected to the output line 122 of the
regulator Z101 through the voltage divider provided by resistors R373 and R374.
This coprocessor chip Z064 is used in this particular instance to sense the
presence or absence of the 12-volt voltage level at the VPP port of **flash**
memory chip Z179 for diagnostic purposes.

Detailed Description Text - DETX (23):

Referring to FIG. 5, a schematic diagram of the plug-in module 32 is shown.
The plug-in module 32 includes a first **EPROM** 142 which contains the exact
computer **program** code that is to be downloaded from the diagnostic tool 28 to
the non-volatile memory of the appropriate on-board vehicle computer circuit.
This particular **EPROM** chip preferably has the same **storage** density (e.g., 32Kx8
or 64Kx8) as the non-volatile memory contained in the on-board vehicle computer
circuit. The plug-in module 32 also includes another **EPROM,** identified by
reference numeral 144, which contains the software necessary to **reprogram** the
non-volatile memory of the on-board vehicle computer circuit. Accordingly,
EPROM 144 contains the operating system for the diagnostic unit 28 and the
algorithms necessary to **reprogram** the on-board non-volatile memory. This
particular **EPROM** will also include a table of part numbers that the new
computer **program** code will supersede. As part of the **reprogramming** method
according to the present invention, **reprogramming** will not be allowed unless
the part number of the on-board vehicle computer circuit is listed in the table

stored in the EPROM 144. Thus, for example, in the case of the engine controller 12, the part number will provide a precise indication of the type of engine involved and the version of the software currently **stored in flash** memory Z179. In this regard, it should be noted that this part number is preferably **stored** in the internal **EEPROM** memory of the microprocessor chip Z144. It should also be noted that either or both of the **EPROMs** contained in the plug-in module 32 may be comprised of any suitable non-volatile memory device, such as a **flash** memory. Additionally, it may be possible to also combine the functions of these two **EPROMs** into a single memory device in the appropriate application.

Detailed Description Text - DETX (25):
Referring to FIGS. 6A and 6B, a flow chart is presented which illustrates the methodology of the present invention in terms of the computer **program** instructions that are **stored** in the non-volatile memory 148 of the plug-in module 32. In this regard, the flow chart of FIGS. 6A-B is specifically directed to the process of **reprogramming the flash** memory chip Z179 in the engine controller 12. While there are variations in this methodology for the purpose of **reprogramming** the non-volatile memory in certain transmission controllers, these variations will be discussed after the preferred process for **reprogramming the flash** memory chip Z179 of the engine controller 12 has been described.

Detailed Description Text - DETX (28):
Once the bootstrap mode is verified, the diagnostic tool 28 will download a series of **programs** (one at a time) to the random access

memory (RAM) within the
microprocessor chip Z144 via the SCIRX receive line. As part of this process,
each byte of the computer **programs** being sent to the vehicle will be echoed or
transmitted back to the computer circuit 152 in the diagnostic tool 28 to
verify the correct reception of the computer **program** instructions. In this
regard, the SCITX transmit line shown in FIG. 2 is used by the microprocessor
chip Z144 to echo back each computer word or byte to the computer circuit 152.
It should also be noted that none of the computer **programs** used in the
reprogramming operation are **stored** on-board the vehicle 10. This feature of
the preferred method serves to enhance the security of the computer **program**
instructions **stored in the flash** memory chip Z179 of the engine controller 12.

Detailed Description Text - DETX (30):
Block 212 indicates that the diagnostic tool 22 will then transmit a part
number **program** to the microprocessor chip Z144. The part number **program** is
used to read the existing part number of the engine controller 12 from the
flash memory chip Z179. Block 214 then shows that the part number **program** will
be executed by the microprocessor chip Z144. As indicated by block 215 the
diagnostic tool 28 will compare the part number received with its **stored** table
of part numbers for which the **reprogramming** operation will be permitted. This
feature of the present invention will insure that the proper plug-in module 32
is being used for the particular non-volatile memory chip contained in the
on-board vehicle computer circuit. This feature of the present invention could
also be used to avoid the need to **reprogram** the on-board non-volatile memory,
where the memory device already has the most current

version of the software
stored in memory. If a part number match is not found from the engine
controller part number **stored in the flash** memory chip Z179, the part number
program will then read a predefined location in the internal **EEPROM** of the
microprocessor chip Z144 to see if an acceptable part number has been **stored** in
this location. As will be discussed below, the engine controller part number
from the **flash** memory chip Z179 is temporarily **stored** in the internal **EEPROM** of
the microprocessor chip Z144 prior to the step of erasing the contents of the
flash memory chip Z179.

Detailed Description Text - DETX (31):

Block 215 also indicates that the identity of the manufacturer for the **flash**
memory chip Z179 will be read next. In order to read this part identity, the
diagnostic tool 28 will download the manufacturer I.D. routine and then cause
the **reprogramming** command signal to be transmitted to the **flash** memory chip
Z179 via the SCIRX receive line. Once the part identity number is received by
the diagnostic tool 28, blocks 216-217 indicate that the **reprogramming** command
signal will be turned off. This I.D. number is used to determine which erase
and **reprogramming** algorithms should be sent to the microprocessor chip Z144, as
these algorithms may vary with the specific manufacturer or generation of the
flash memory chip Z179.

Detailed Description Text - DETX (32):

In one form of the present invention, it is preferred that the engine
controller part number originally **stored in the flash** memory chip Z179 also be
stored in the EEPROM memory of the microprocessor chip Z144 before the **flash**

memory chip is erased. This provision is used to provide a temporary part
identity reference in the event of a power loss or other **program** interruption
during the erasure sequence. Once the engine controller part number has been
stored, then the memory locations in the **flash** memory chip Z179 may then be
erased. After the **flash** memory chip Z179 has been completely **reprogrammed,**
then the temporary part number reference may be erased from the **EEPROM** memory
of the microprocessor chip Z144.

Detailed Description Text - DETX (33):
Block 218 indicates that the algorithm required to erase the contents of the
flash memory chip Z179 is downloaded from the diagnostic tool 28, and the
reprogramming command signal is again transmitted to unlock the **flash** memory
chip. Block 220 indicates that the erase routine will be performed in
accordance with this algorithm, and diamond 222 indicates that the diagnostic
tool 28 will wait for one of two messages from the microprocessor chip Z144.
Specifically, if the erasure has been completed and verified, the **program** flow
will continue on to **reprogramming** block 224. However, if the erasure operation
was unsuccessful, then an error message will be transmitted, and block 226
shows that the diagnostic tool 28 will inform the technician of the failure via
the display 42.

Detailed Description Text - DETX (34):
Block 224 indicates that the algorithm for **storing** new computer **program** code
(e.g., instructions, data, pointers and the like) and the first 64 bytes of
this code are downloaded from the diagnostic tool 28. The 20 volt
reprogramming command signal is then transmitted to the

flash memory chip Z179 in order to permit the chip to receive and **store** the new computer **program** code.

Detailed Description Text - DETX (35):
Block 226 indicates that the new computer **program** code will be transmitted and **stored** in packets of 64 bytes. As with the transmission of the **reprogramming** algorithms from the diagnostic tool 28, each packet of new computer **program** code will be echoed back to the diagnostic tool to verify the proper **storage** of these bytes in the **flash** memory chip Z179. In this regard, diamond 228 indicates that the diagnostic tool 28 will compare each of the transmitted bytes with the echoed bytes to insure that there is a correct match. If a correct match has not been found for any of the transmitted bytes, then a failure message will be conveyed to the technician via display 42 (block 230).

Detailed Description Text - DETX (36):
Diamond 232 and blocks 234-236 indicate that the diagnostic tool 28 will continue to send the rest of the new computer **program** code to the **flash** memory chip Z179 (through the microprocessor chip Z144) in an iterative, self-checking process. Specifically, blocks 234-236 indicate that the **reprogramming** command signal will be turned off before each packet of new computer **program** code is transmitted, then switched on after each packet has been transmitted, and then the computer circuit 152 in the diagnostic tool 28 will check to insure that each of the transmitted bytes of information in the packet has been successfully received and **stored**.

Detailed Description Text - DETX (38):
With respect to the process of reprogramming the non-volatile memories of other on-board vehicle computer circuits, the process may be the same or close to the preferred process described above for the engine controller 12. However, one factor which could cause a difference in the preferred process has to do with the communication rates provided by the diagnostic tool 28 and the particular on-board vehicle computer circuit whose non-volatile memory is to be reprogrammed. In this regard, the microprocessor chip Z144 has an internal bootstrap algorithm which sets up an initial SCI signal **transfer protocol at a 7812.5 baud** rate in the bootstrap mode. The **baud** rate is then reset to 62.5 kilobaud for the actual transmission of computer programs to the microprocessor chip Z144 from the diagnostic tool 28. These **baud** rates are determined at least in part by the clock speed of the microprocessor chip, and in this particular case, the generation of 68HC11 microprocessor chips used in the engine controller 12 have a clock rate of 2 MHz. The present generation of DRB II units also include a 68HC11 microprocessor in its computer circuit 152. Even though the clock rate of the microprocessor chip in the DRB II unit is 1 MHz, the initial SCI signal **transfers are set for the 7812.5 baud** rate. Accordingly, it should be appreciated that there is synchronization between the initial SCI **baud rates for communication** between the DRB II unit and the microprocessor chip Z144 in the engine controller.

Detailed Description Text - DETX (39):
However, an incompatibility between the **communication baud** rates could arise, for example, if the clock rate of the on-board vehicle computer circuit were changed. Specifically, if the clock rate of the

68HC11 microprocessor
chip was increased to 3 MHz (i.e., a 50% increase), then the initial **baud** rate
of the this on-board computer chip could also increase proportionally to
11,718.75 **baud** in the bootstrap mode. In this regard, certain transmission
controllers 14 may employ such an increased clock rate. While the special test
mode could be used in the place of the bootstrap mode as an initial step of the
reprogramming process, since the special test mode could permit compatible **baud**
rates, the special test mode of the microprocessor chip Z144 would not be as
advantageous as the bootstrap mode. This is because the **program** needed by the
microprocessor chip Z144 to permit initial communication with the diagnostic
tool would have to be derived from the on-board **EEPROM** memory and loaded into
the internal RAM memory of the microprocessor chip Z144. In contrast, the
communication **program** for the bootstrap mode is contained in the internal **ROM**
memory of the microprocessor chip Z144. Thus, if there was a loss of power
during communication in the test mode, the ability to communicate with the
diagnostic tool 28 would be lost, and the process would have to be restarted
from the beginning.

Detailed Description Text - DETX (40):
Accordingly, it is preferred that the bootstrap mode still be utilized. If
the microprocessor chip employed in the vehicle cannot communicate at the **baud**
rate of the signals transmitted by the diagnostic tool 28, then the on-board
microprocessor chip will interpret the incorrect **baud** rate as a command to
execute a series of instructions from its on-board **EEPROM** memory which will
adjust the microprocessor's **baud** rate to that supplied by the diagnostic tool.

The microprocessor will then jump back to the normal bootstrap mode with the new **baud** rate, and the **reprogramming** process will proceed as described above.

Claims Text - CLTX (23):

15. The method according to claim 11, wherein said non-volatile memory is comprised of at least one **flash** memory chip and substantially the entire contents of said **flash** memory chip are erased before said new computer **program** code is transmitted.

Current US Cross Reference Classification - CCXR (2):

701/35